multiLane

ML4062-LB2a-112

Technical Reference

QSFP-DD800 Electrical Passive Loopback Module

CMIS 4.0 Compliant

Innovation for the next generation

Table of Contents

1 Overview

The **ML4062-LB2a-112** provides a straightforward method to test QSFP-DD800 ports at every level of the switch production process. The electrical loopback (ELB) acts as a fully featured QSFP-DD800 transceiver and is used for testing QSFP-DD800 transceiver switch ports during physical layer tests and system bring-up. Ideal for R&D validation, production testing, and field testing, the **ML4062-LB2a-112** follows the **CMIS Rev 4.0** standard and is packaged in standard MSA housing compatible with all QSFP-DD power classes.

1.1 ML4062-LB2a-112 QSFP-DD800 Thermal Load | Key Features

- QSFP-DD800 MSA Form Factor
- Operating up to 112G per lane
- MSA Compatible Configuration and EEPROM
- Programmable MSA memory pages
- Custom memory maps
- I2C Interface
- I2C control from edge connectors and from rear pin header
- Controller card with I2C Master, supports multiple modules, USB master
- Hot Pluggable module
- Eleven independent power spots dissipating up to 30 W
- Four temperature sensors
- Voltage sensor
- Current sensor
- Temperature Monitor and alarms warning
- Cut-off temperature preventing module overheating

1.2 Recommended Operating Conditions

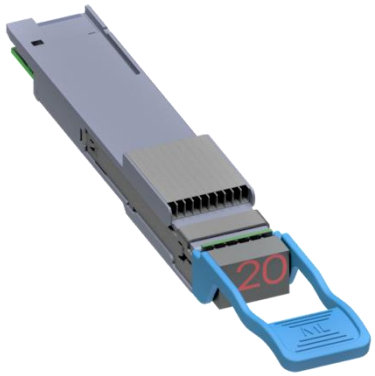
Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		-40		105	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		30	W

2 Ordering Information

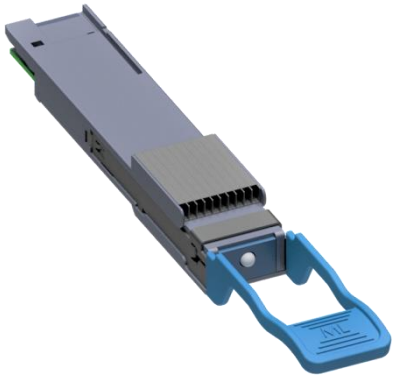
2.1 Ordering Options

In addition to full features of QSFP-DD, the **ML4062-LB2a-112** provides additional options depending on your requirements and pre-ordering information, as detailed in the table below:

Option	Part Number	Description
#1 - LCD Display	ML4062-LB2a-112 -LCD	Temperature and other Monitoring values
#2 - LED Indicator	ML4062-LB2a-112-LED	Power Mode and Alarms Monitoring
#3 - Pin Header	ML4062-LB2a-112-CON	Board to Board Connection



LCD Display (R&D)



LED Indicator (Mass Production)

Pin Header (Thermal Dissipation/Diagnostics)

In options 1 and 2, the module should be inserted from the edge card (module paddle) into a QSFP-DD host connector. The **ML4062-LB2a-112-LED** displays the module's state as detailed in section 2.2. The **ML4062-LB2a-112-LCD** can then display temperature or any other monitoring value as detailed in section 2.3.

With the **ML4062-LB2a-112-CON**, in addition to the insertion method and control described above, the module can also be inserted into a controller board from the front pin header connector, providing power and allowing I2C communication with the controller board, as detailed in section 2.4.

2.2 LED Indicator

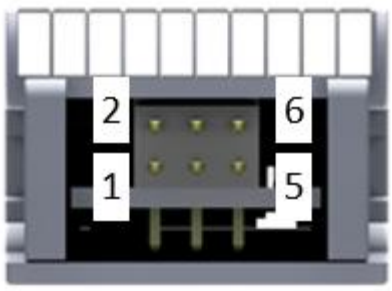
Green (Solid) – Module is in high power mode.
Red (Solid) – Module is in low power mode.
Green (Blinking) – Module is in high power mode and Voltage or Temperature Alarm is triggered.
Red (Blinking) – Module in low power mode and Voltage or Temperature Alarm is triggered.

2.3 LCD Display

The LCD can display various monitoring values depending on the LCD control register. It can indicate whether module is in LOW power state, HIGH power state, or Interrupt. The text orientation displayed on the LCD is also controllable. Refer to section 3.5.12 for more details on LCD Control register and functionality.

2.4 Pin Header

The Pin header connector mapping is shown below:



Connector Front View

Pin #	Description
1 - 5	GND
4 - 6	3.3 V
2	I2C-SCL
3	I2C-SDA

3 Functional Description

3.1 Management Data Interface – I2C

The **ML4062-LB2a-112** supports the I2C interface.

3.2 I2C Signals, Addressing and Frame Structure

3.2.1 I2C Frame

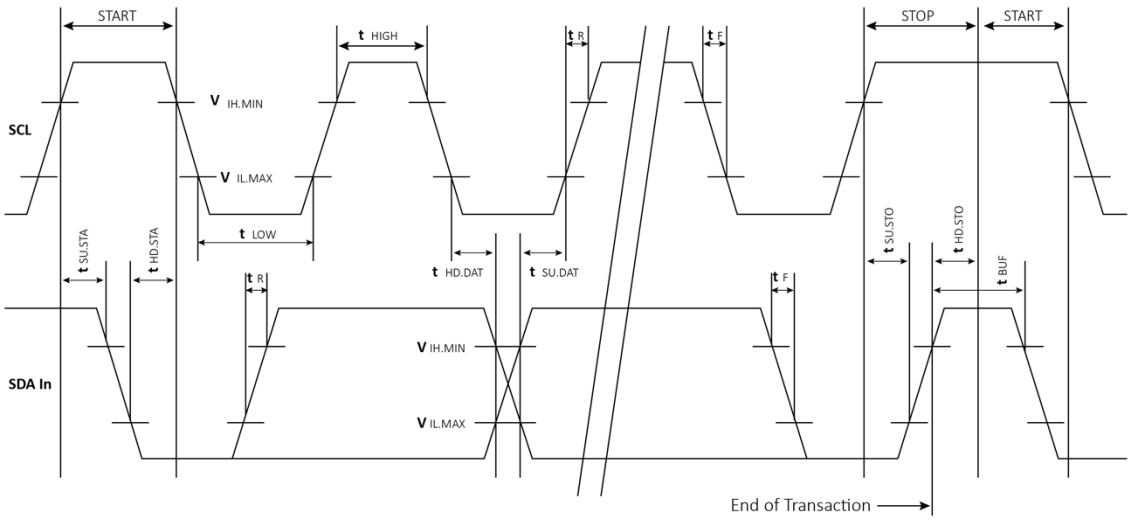


Figure 1: QSFP-DD Timing Diagram

Before initiating a 2-wire serial bus communication, provide setup time on the ModSelL line of all modules on the 2-wire bus. Do not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h).

In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module does not respond to or accept 2-wire serial bus instructions unless it is selected.

3.2.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in the table below:

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{SCL}	10		400	kHz
Clock Pulse Width Low	t_{LOW}	550			ns
Clock Pulse Width High	t_{High}	550			ns
Time bus free before new transmission can start	t_{BUF}	1			us
START Hold Time	$t_{HD.STA}$	550			ns
START Set-up Time	$t_{SU.STA}$	550			ns
Data In Hold Time	$t_{HD.DAT}$		250		ns
Data in Set-up Time	$t_{SU.DAT}$		500		ns
STOP Set-up Time	$t_{SU.STO}$	600			ns
ModSelL Setup Time	$t_{SU.ModSelL}$	1			ms
ModSelL Hold Time	$T_{HD.ModSelL}$	10			us

3.2.3 Memory Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		10		us
Complete Single Write	tWR	5			ms

QSFP-DD memory transaction timings are given in the above table.

3.2.4 Device Addressing and Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP-DD in 8-bit words. Every Byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.

Memory (Management Interface) Reset: After an interruption in protocol, power loss, or system reset, the QSFP-DD Module management interface can be reset. Memory reset is intended *only* to reset the QSFP-DD transceiver management interface (to correct a hung bus). No other module functionality is implied.
Clock up to 9 cycles.
Look for SDA high in each cycle while SCL is high.
Create a Start condition as SDA is high.
After an interruption in protocol, power loss, or system reset, the QSFP-DD Module management interface can be reset. Memory reset only resets the QSFP-DD transceiver management interface (to correct a hung bus) leaving all other module functionality intact.
Clock up to 9 cycles.
Look for SDA high in each cycle while SCL is high.
Create a Start condition as SDA is high.

Device Addressing: QSFP-DD devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 2. This is common to all QSFP-DD devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: QSFP-DD Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP-DD Module will output a zero (ACK) on the SDA line to acknowledge the address.

3.3 QSFP-DD Memory Map

3.3.1 Full Map

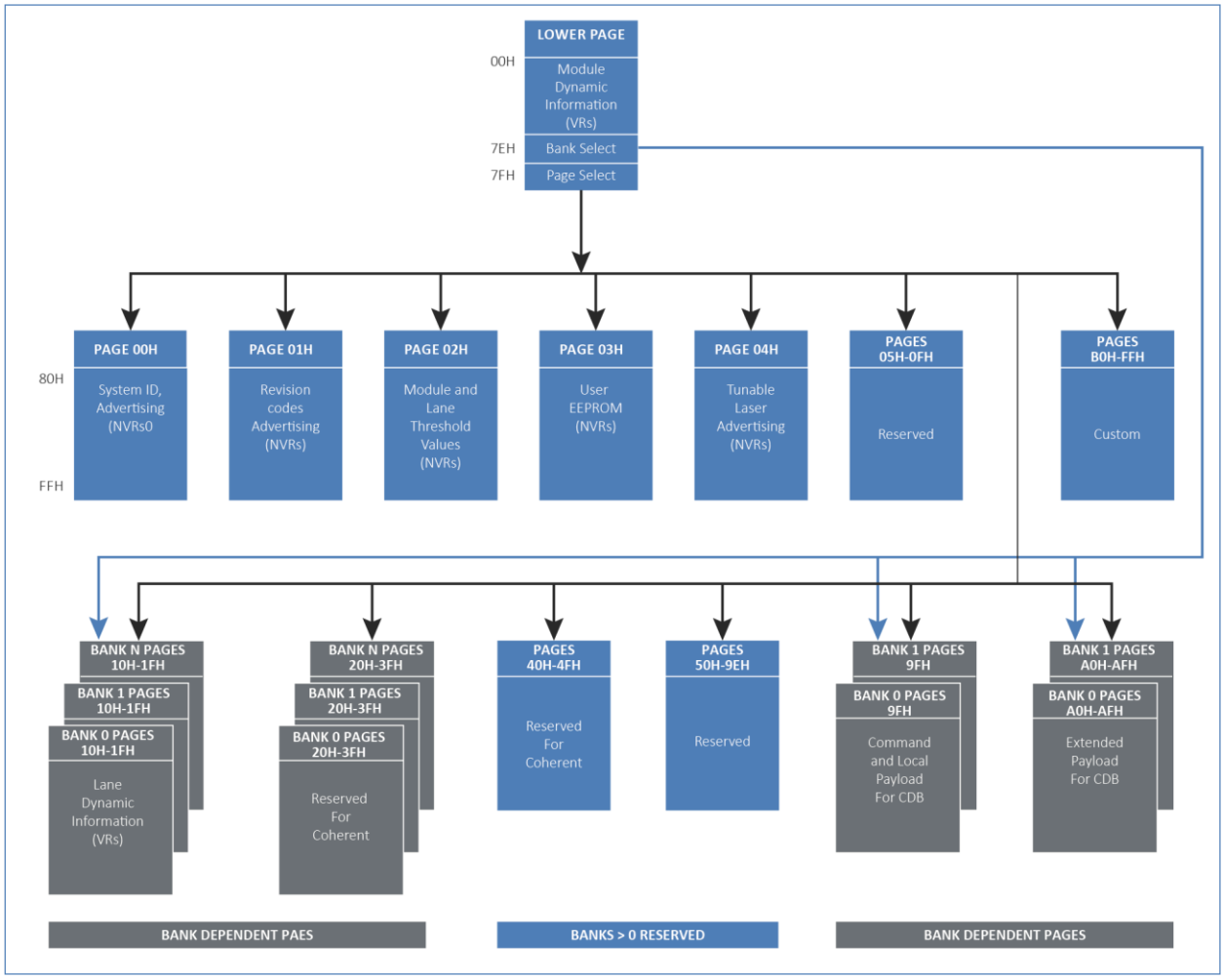


Figure 3: QSFP-DD Memory Map

This section defines the Memory Map for QSFP-DD transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices. The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

3.3.2 ML4062-LB2a-112 Memory Map

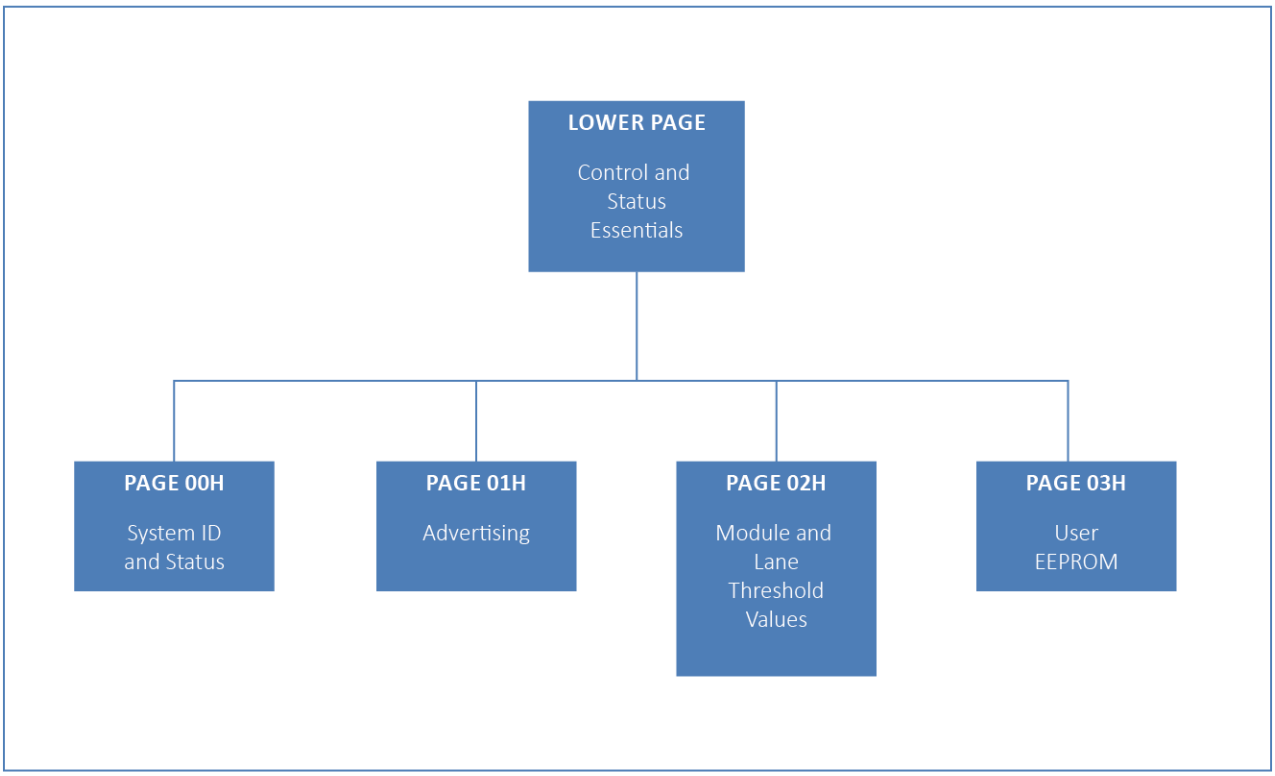


Figure 4: Implemented Memory Map

3.3.3 Memory Content

The table below shows the memory content.

Address	Hex	Decimal	ASCII	MSA Description
LowMem 0(00h)	0x18	24		Identifier
LowMem 1(01h)	0x40	64	@	Revision Compliance
LowMem 2(02h)	0x00	0		Flat-mem / TWI Max Speed
LowMem 3(03h)	0x00	0		Module State / Software interrupt
LowMem 4(04h)	0x00	0		Bank 0 flag summary
LowMem 5(05h)	0x00	0		Bank 1 flag summary
LowMem 6(06h)	0x00	0		Bank 2 flag summary
LowMem 7(07h)	0x00	0		Bank 3 flag summary
LowMem 8(08h)	0x00	0		Data Path/Module FW fault and Module State changed flag
LowMem 9(09h)	0x00	0		Latched VCC3.3/Temp Alarm and Warning
LowMem 10(0Ah)	0x00	0		Latched AUX1/2 Alarm and Warning

LowMem 11(0Bh)	0x00	0		Latched Vendor Defined/AUX3 Alarm and Warning
LowMem 12(0Ch)	0x00	0		Reserved
LowMem 13(0Dh)	0x00	0		Custom
LowMem 14(0Eh)				Internally measured Temperature T.S.4 MSB
LowMem 15(0Fh)				Internally measured Temperature T.S.4 LSB
LowMem 16(10h)				Internally measured Supply 3.3v MSB
LowMem 17(11h)				Internally measured Supply 3.3v LSB
LowMem 18-23 (12h-17h)	0x00	0		
LowMem 24(18h)				Internally measured current MSB
LowMem 25(19h)				Internally measured current LSB
LowMem 26(1Ah)	0x40	64	@	Software reset / Low power control
LowMem 27-38 (1Bh-26h)	0x00	0		
LowMem 39(27h)	0x01	1		Major FW Rev
LowMem 40(28h)	0x00	0		Minor FW Rev
LowMem 41-125 (29h-7Dh)	0x00	0		
LowMem 126(7Eh)	0x00	0		Bank Select Byte
LowMem 127(7Fh)	0x00	0		Page Select Byte
Page00 128(80h)	0x18	24		Identifier
Page00 129(81h)	0x4D	77	M	Vendor Name
Page00 130(82h)	0x55	85	U	Vendor Name
Page00 131(83h)	0x4C	76	L	Vendor Name
Page00 132(84h)	0x54	84	T	Vendor Name
Page00 133(85h)	0x49	73	I	Vendor Name
Page00 134(86h)	0x4C	76	L	Vendor Name
Page00 135(87h)	0x41	65	A	Vendor Name
Page00 136(88h)	0x4E	78	N	Vendor Name
Page00 137(89h)	0x45	69	E	Vendor Name
Page00 138(8Ah)	0x20	32		Vendor Name
Page00 139(8Bh)	0x20	32		Vendor Name
Page00 140(8Ch)	0x20	32		Vendor Name

Page00 141(8Dh)	0x20	32		Vendor Name
Page00 142(8Eh)	0x20	32		Vendor Name
Page00 143(8Fh)	0x20	32		Vendor Name
Page00 144(90h)	0x20	32		Vendor Name
Page00 145(91h)	0x00	0		Vendor OUI
Page00 146(92h)	0x00	0		Vendor OUI
Page00 147(93h)	0x00	0		Vendor OUI
Page00 148(94h)	0x4D	77	M	Vendor PN
Page00 149(95h)	0x4C	76	L	Vendor PN
Page00 150(96h)	0x34	52	4	Vendor PN
Page00 151(97h)	0x30	48	0	Vendor PN
Page00 152(98h)	0x36	54	6	Vendor PN
Page00 153(99h)	0x32	50	2	Vendor PN
Page00 154(9Ah)	0x2D	45	-	Vendor PN
Page00 155(9Bh)	0x4C	76	L	Vendor PN
Page00 156(9Ch)	0x42	66	B	Vendor PN
Page00 157(9Dh)	0x32	50	2	Vendor PN
Page00 158(9Eh)	0x61	97	a	Vendor PN
Page00 159(9Fh)	0x2D	45	-	Vendor PN
Page00 160(A0h)	0x31	49	1	Vendor PN
Page00 161(A1h)	0x31	49	1	Vendor PN
Page00 162(A2h)	0x32	50	2	Vendor PN
Page00 163(A3h)	0x20	32		Vendor PN
Page00 164(A4h)	0x31	49	1	Vendor Rev
Page00 165(A5h)	0x30	48	0	Vendor Rev
Page00 166(A6h)	0x20	32		Vendor SN
Page00 167(A7h)	0x20	32		Vendor SN
Page00 168(A8h)	0x20	32		Vendor SN
Page00 169(A9h)	0x20	32		Vendor SN
Page00 170(AAh)	0x20	32		Vendor SN

Page00 171(ABh)	0x20	32		Vendor SN
Page00 172(ACh)	0x20	32		Vendor SN
Page00 173(ADh)	0x20	32		Vendor SN
Page00 174(AEh)	0x20	32		Vendor SN
Page00 175(AFh)	0x20	32		Vendor SN
Page00 176(B0h)	0x20	32		Vendor SN
Page00 177(B1h)	0x02	32		Vendor SN
Page00 178(B2h)	0x20	32		Vendor SN
Page00 179(B3h)	0x20	32		Vendor SN
Page00 180(B4h)	0x20	32		Vendor SN
Page00 181(B5h)	0x20	32		Vendor SN
Page00 182(B6h)	0x31	49	1	Date Code
Page00 183(B7h)	0x39	57	9	Date Code
Page00 184(B8h)	0x30	48	0	Date Code
Page00 185(B9h)	0x35	53	5	Date Code
Page00 186(BAh)	0x31	49	1	Date Code
Page00 187(BBh)	0x34	52	4	Date Code
Page00 188(BCh)	0x30	48	0	Date Code
Page00 189(BDh)	0x31	49	1	Date Code
Page00 190(BEh)	0x00	0		CLEI Code
Page00 191(BFh)	0x00	0		CLEI Code
Page00 192(C0h)	0x00	0		CLEI Code
Page00 193(C1h)	0x00	0		CLEI Code
Page00 194(C2h)	0x00	0		CLEI Code
Page00 195(C3h)	0x00	0		CLEI Code
Page00 196(C4h)	0x00	0		CLEI Code
Page00 197(C5h)	0x00	0		CLEI Code
Page00 198(C6h)	0x00	0		CLEI Code
Page00 199(C7h)	0x00	0		CLEI Code
Page00 200(C8h)	0xE0	224	?	Module Power Characteristics

Page00 201(C9h)	0x78	120	x	Module Power Characteristics
Page00 202(CAh)	0x00	0		Cable assembly length
Page00 203(CBh)	0x00	0		Media Connector Type
Page00 204(CCh)	0x01	1		Copper Cable Attenuation
Page00 205(CDh)	0x01	1		Copper Cable Attenuation
Page00 206(CEh)	0x02	2		Copper Cable Attenuation
Page00 207(CFh)	0x03	3		Copper Cable Attenuation
Page00 208(D0h)	0x00	0		Copper Cable Attenuation
Page00 209(D1h)	0x00	0		Copper Cable Attenuation
Page00 210(D2h)	0x00	0		Cable Assembly Lane Information
Page00 211(D3h)	0x00	0		Cable Assembly Lane Information
Page00 212(D4h)	0x00	0		Media Interface Technology
Page00 213-220 (D5h-DCh)	0x00	0		Reserved
Page00 221(DDh)	0x00	0		Custom
Page00 222(DEh)				Checksum
Page00 223-255 (DFh-FFh)	0x00	0		Custom Info NV
Page01 128(80h)	0x00	0		Inactive Major FW Rev
Page01 129(81h)	0x00	0		Inactive Minor FW Rev
Page01 130(82h)	0x01	1		Module Major HW Rev
Page01 131(83h)	0x00	0		Module Minor HW Rev
Page01 132(84h)	0x00	0		link length SMF
Page01 133(85h)	0x00	0		link length (OM5)
Page01 134(86h)	0x00	0		link length (OM4)
Page01 135(87h)	0x00	0		link length (OM3)
Page01 136(88h)	0x00	0		link length (OM2)
Page01 137(89h)	0x00	0		Reserved
Page01 138(8Ah)	0x00	0		Nominal Wavelength
Page01 139(8Bh)	0x00	0		Nominal Wavelength
Page01 140(8Ch)	0x00	0		Wavelength Tolerance
Page01 141(8Dh)	0x00	0		Wavelength Tolerance

Page01 142(8Eh)	0x04	4		Implemented Management Interface features advertising
Page01 143(8Fh)	0xDF	223	?	Implemented Management Interface features advertising
Page01 144(90h)	0x00	0		Implemented Management Interface features advertising
Page01 145(91h)	0x00	0		Module Characteristics advertising
Page01 146(92h)	0x55	85	U	Module Characteristics advertising
Page01 147(93h)	0xD8	216	?	Module Characteristics advertising
Page01 148(94h)	0x00	0		Module Characteristics advertising
Page01 149(95h)	0x00	0		Module Characteristics advertising
Page01 150(96h)	0x91	145	?	Module Characteristics advertising
Page01 151(97h)	0x00	0		Module Characteristics advertising
Page01 152(98h)	0x00	0		Module Characteristics advertising
Page01 153(99h)	0x00	0		Module Characteristics advertising
Page01 154(9Ah)	0x00	0		Module Characteristics advertising
Page01 155(9Bh)	0x00	0		Implemented Controls advertising
Page01 156(9Ch)	0x00	0		Implemented Controls advertising
Page01 157(9Dh)	0x00	0		Implemented Flags advertising
Page01 158(9Eh)	0x00	0		Implemented Flags advertising
Page01 159(9Fh)	0x23	35	#	Implemented Monitors advertising
Page01 160(A0h)	0x00	0		Implemented Monitors advertising
Page01 161(A1h)	0x00	0		Implemented Signal Integrity Controls advertising
Page01 162(A2h)	0x00	0		Implemented Signal Integrity Controls advertising
Page01 163-254 (A3h-FEh)	0x00	0		
Page01 255(FFh)				Checksum
Page02 128(80h)	0x5F	95	_	Temperature monitor high alarm threshold MSB
Page02 129(81h)	0x00	0		Temperature monitor high alarm threshold LSB
Page02 130(82h)	0x00	0		Temperature monitor low alarm threshold MSB
Page02 131(83h)	0x00	0		Temperature monitor low alarm threshold LSB
Page02 132(84h)	0x55	85	U	Temperature monitor high warning threshold MSB
Page02 133(85h)	0x00	0		Temperature monitor high warning threshold LSB
Page02 134(86h)	0x05	5		Temperature monitor low warning threshold MSB

Page02 135(87h)	0x00	0		Temperature monitor low warning threshold LSB
Page02 136(88h)	0x8C	140	?	Supply 3.3-volt monitor high alarm threshold MSB
Page02 137(89h)	0xA0	160	?	Supply 3.3-volt monitor high alarm threshold LSB
Page02 138(8Ah)	0x75	117	u	Supply 3.3-volt monitor low alarm threshold MSB
Page02 139(8Bh)	0x30	48	0	Supply 3.3-volt monitor low alarm threshold LSB
Page02 140(8Ch)	0x8A	138	?	Supply 3.3-volt monitor high warning threshold MSB
Page02 141(8Dh)	0xAC	172	?	Supply 3.3-volt monitor high warning threshold LSB
Page02 142(8Eh)	0x77	119	w	Supply 3.3-volt monitor low warning threshold MSB
Page02 143(8Fh)	0x24	36	$	Supply 3.3-volt monitor low warning threshold LSB
Page02 144-254 (90h-FEh)	0x00	0		
Page02 255(FFh)				Checksum
Page03 129(81h)				LCD Control Register
Page03 130(82h)				LCD Presence
Page03 131(83h)	0x00	0		User EEPROM
Page03 132(84h)				Insertion Counter MSB
Page03 133(85h)				Insertion Counter LSB
Page03 134(86h)	0x64	100	d	Cut-Off temperature
Page03 135(87h)				Power control registers
Page03 136(88h)				
Page03 137(89h)				
Page03 138(8Ah)				
Page03 139(8Bh)	0x00	0		User EEPROM
Page03 140(8Ch)				
Page03 141(8Dh)				LPMode/ModSelL State/Edge Detection
Page03 142(8Eh)				IntL Control Register
Page03 143(8Fh)	0x00	0		User EEPROM NVR
Page03 144(90h)	0x00	0		User EEPROM NVR
Page03 145(91h)	0x00	0		User EEPROM NVR
Page03 146(92h)	0x00	0		User EEPROM NVR
Page03 147(93h)	0x00	0		User EEPROM NVR

Page03 148(94h)	0x00	0		User EEPROM NVR
Page03 149(95h)	0x00	0		User EEPROM NVR
Page03 150(96h)				Internally measured module temperature 1 MSB
Page03 151(97h)				Internally measured module temperature 1 LSB
Page03 152(98h)				Internally measured module temperature 2 MSB
Page03 153(99h)				Internally measured module temperature 2 LSB
Page03 154(9Ah)				Internally measured module temperature 3 MSB
Page03 155(9Bh)				Internally measured module temperature 3 LSB
Page03 156-254 (9Ch-FEh)	0x00	0		User EEPROM

3.3.4 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03	128-129	RW (NVR)
	130	RO
	131	RW (NVR)
	132-133	RO
	134-140	RW (NVR)
	141	RW
	142-149	RW (NVR)
	150-155	RO
	156-255	RW (NVR)

3.4 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModselL

- ResetL
- LPMode
- IntL
- ModPrstL

3.4.1 ModselL

The ModSelL is an input signal to the module that is pulled up to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host.

3.4.2 ResetL

ResetL, is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset.

3.4.3 LPMode

LPMode is an input signal to the module from the host, operating with active high logic. The LPMode signal is pulled up to Vcc in the QSFP-DD module through a 4.75 kOhm resistor. The LPMode signal intervenes in the Module State Transition (refer to section 3.5.2 for more details).

3.4.4 IntL

IntL is an output signal. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The IntL signal is de-asserted "High" after all set interrupt flags are read (IntL pin is open drain, it is pulled high by a pull-up resistor on the Host side).

3.4.5 ModPrstL

ModPrsL is grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and reasserted "High" when the module is physically absent from the host connector.

3.5 ML4062-LB2a-112 Specific Functions

3.5.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4062-LB2a-112** implements two module states: ModuleLowPwr and ModuleReady.
The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode, where the Power Spots are

deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

3.5.2 Module State Transition

The state transition between Low-Power and High-Power is related to three parameters:

1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for low-power and high-power state are summarized in the table below.

ForceLowPwr (Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

3.5.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
26 (lower Page)	6	LowPwr	Parameter used to control the module power mode (refer to section 3.5.2) Default value =1	RW
	4	ForceLowPwr	0b = high power mode(default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b = not in reset 1b = Software reset	
3 (lower page)	0	Software	Digital state of Interrupt:	RO

		Interrupt	0b = Interrupt source is present 1b = No interrupt source present	

3.5.4 Temperature Monitor

The **ML4062-LB2a-112** has 4 internal temperature sensors, two on the PCBA and two others on the shell in order to continuously monitor the module temperature. Internally measured Module temperatures are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127° C to +128° C that is considered valid between –40° and +125° C.

Address	Bit	Name	Description	Type
14 Lower page	All	Temperature MSB	Internally measured TempSense4 (shell T.S.)	RO
15 Lower page	All	Temperature LSB	Internally measured TempSense4 (shell T.S.)	
150 Page 03	All	Temperature MSB	Internally measured TempSense1 (PCB Bottom)	
151 Page 03	All	Temperature LSB	Internally measured TempSense1 (PCB Bottom)	
152 Page 03	All	Temperature MSB	Internally measured TempSense2 (shell T.S.)	
153 Page 03	All	Temperature LSB	Internally measured TempSense2 (shell T.S.)	
154 Page 03	All	Temperature MSB	Internally measured TempSense3 (PCB Bottom)	
155 Page 03	All	Temperature LSB	Internally measured TempSense3 (PCB Bottom)	

The distribution of internal temperature sensors is shown in the figure.

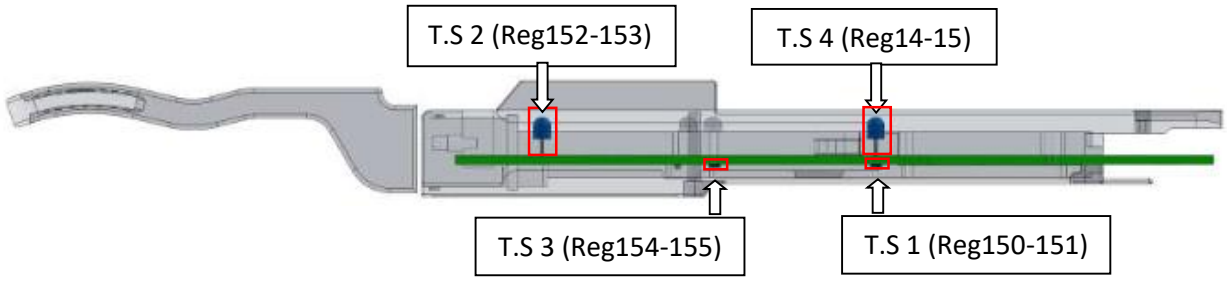


Figure 5: Temperature sensor location

The temperature Alarms' and warnings' interrupt flags exist in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

3.5.5 Voltage Sense

A voltage sense circuit is available in the **ML4062-LB2a-112** that allows to measure the internal module supplied voltage Vcc, with LSB unit is 0.1 mV.

Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage	RO
17	All	Supply voltage LSB	Internally measured supply voltage	

The Voltage Alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

3.5.6 Current Sense

A current sense circuit is available in the **ML4062-LB2a-112** that allows monitoring the current consumption of the heaters that are distributed over ten power spots. The current is stored in low memory registers 24 and 25. The current sense is able to measure up to 7.17 A.
Note that the Max current consumption of the module is 9.1 A, but the current sense can read only up to 7.17 A.

Address	Bit	Name	Description	Type
24	All	Current Consumption MSB	Current consumption in mA	RO
25	All	Current Consumption LSB		

3.5.7 Programmable Power Dissipation and Thermal Emulation

The **ML4062-LB2a-112** module contains eleven thermal spots positioned as shown in Figure 6, to allow the user to emulate the thermal behavior of an optical module.

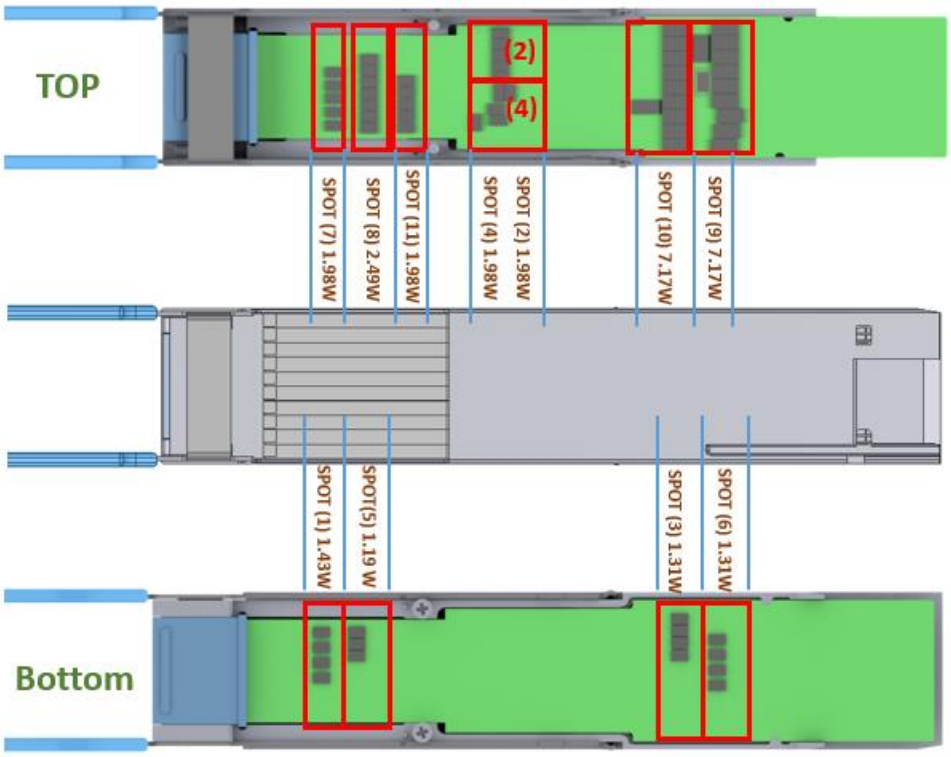


Figure 6: Thermal spots distribution

While some of these spots are PWM controlled, others are ON/OFF controlled. The table below shows control type for each of these thermal spots.

Power Spot number	Control Type
5	PWM
1-2-3-4-6-7-8-9-10-11	ON/OFF

Registers 135, 136 and 137, page 03h are used to control thermal spots over I2C. They are 8 bits data wide registers.
The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low-power mode the module automatically turns off all power spots. The values written in these registers are permanently stored.

The control registers of the thermal spots are shown in the table below:

Power Spot	Register	Bit	Power Consumption	Control Type	Memory Type
5	135	7:0	1.19 W	PWM	RW (NVR)
1	136	0	1.43 W	ON/OFF	
2		1	1.98 W		
3		2	1.31 W		
4		3	1.98 W		

6		4	1.31 W		
7		5	1.98 W		
8		6	2.49 W		
9		7	7.17 W		
10	137	0	7.17 W		
11		1	1.98 W		

The Figure 7 shows a side view of the distribution of thermal spots and TIM. Red shapes are the heat spots at the top and bottom of the PCB, and the yellow shapes are TIM for heat conduction to the shell. The TIM conductivity is 3 W/m.K.

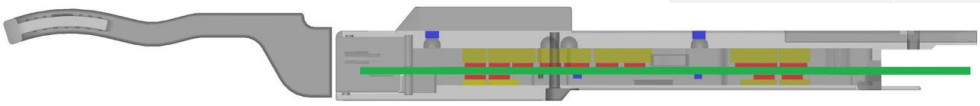


Figure 7: Module side view

3.5.8 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, all power spots will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
The **ML4062-LB2a-112** is set to its maximum Cut-Off temperature of 100˚C by default, and can be programmed to any value from register 134 of memory page 03.

Address	Bit	Name	Description	Type
134	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

3.5.9 Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 page 03.

Address	Bit	Name	Description	Type
132 (page 03)	MSB	Insertion Counter MSB		RO
133 (page 03)	LSB	Insertion Counter LSB	LSB unit = 1 insertion	

3.5.10 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow you to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128(page 02)	ALL	high temp alarm threshold (MSB)	95˚C	RO
129(page 02)	ALL	high temp alarm threshold (LSB)		
130(page 02)	ALL	low temp alarm threshold (MSB)	0° C	
131(page 02)	ALL	low temp alarm threshold (LSB)		
132(page 02)	ALL	high temp warning threshold (MSB)	85˚C	
133(page 02)	ALL	high temp warning threshold (LSB)		
134(page 02)	ALL	low temp warning threshold (MSB)	5˚C	
135(page 02)	ALL	low temp warning threshold (LSB)		
136(page 02)	ALL	high volt alarm threshold (MSB)	3.6 V	
137(page 02)	ALL	high volt alarm threshold (LSB)		
138(page 02)	ALL	low volt alarm threshold (MSB)	3.0 V	
139(page 02)	ALL	low volt alarm threshold (LSB)		
140(page 02)	ALL	high volt warning threshold (MSB)	3.55 V	
141(page 02)	ALL	high volt warning threshold (LSB)		
142(page 02)	ALL	low volt warning threshold (MSB)	3.05 V	
143(page 02)	ALL	low volt warning threshold (LSB)		

3.5.11 FW and HW Revision

Information about the FW and HW revision are present in Lower Page, registers 39-40, and in page 01 registers 130-131, respectively, as described in the table below.

Address	Bit	Description	Type
39 (Lower Page)	All	Major FW Rev	RO
40 (Lower Page)	All	Minor FW Rev	
130 (page 01)	All	Major HW Rev	
131 (page 01)	All	Minor HW Rev	

3.5.12 LCD Display

This section describes the LCD functionality; only available for Part Number: **ML4062-LB2a-112-LCD**.
The LCD is used to display various monitoring variables. The displayed variables are controlled form address 129 bit1:0, page 03, where one of three variables can be displayed on the LCD as detailed below.
Also, the text orientation displayed on the LCD is controllable from address 129 bit 4, page 03.

Address	Bit	Name	Description	Type
129 (page 03)	1~0	LCD Control Register	Monitoring Variable Control: 00b: Temperature (Temp sense 4 reported in registers 14-15) 01b: Voltage (reported in registers 16-17) 10b: Current (reported in registers 24-25)	RW (NVR)
	4		Text orientation: 0b: Normal 1b: Inverted	

The displayed variables are described below:

- Temperature: the displayed temperature is same as the one reported in addresses 14-15 that report the readings from temperature sensor 4 that is attached to the shell. The displayed temperature always refers to Temp Sense 4, and cannot be changed.
- Voltage: the displayed voltage refers to the module voltage net that is reported in addresses 16-17.
- Current: the displayed current refers to the monitored current that is reported in addresses 24-25.

The LCD indicates whether module is in LOW-power state, HIGH-power state, or Interrupt as follows:

- Low-power state: the DOT of the right digit is ON.
- High-power state: the DOT of the right digit is OFF.
- Interrupt: the value on the display is BLINKING (indicating an alarm is triggered).

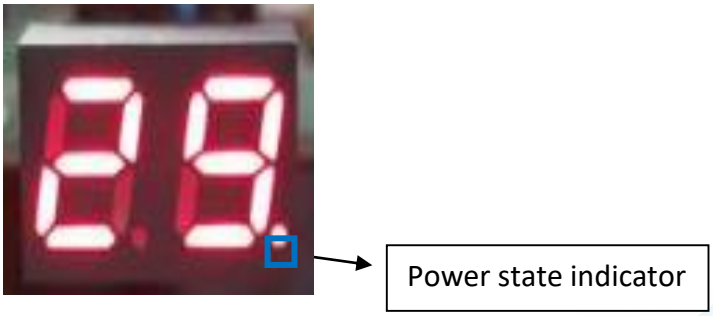


Figure 8: LCD Display

3.5.13 Status Register

Register 141 of page 3 reports the digital state of the QSFP-DD low speed signals.

acx	Bit	Name	Description	Type
141 (page 03)	0	ModSel	Digital state of ModSel pin	RO
	1	LPMode	Digital state of LPMode	

Note that when the ModSelL is High the I2C will stop working and the user will read FF from register 141.

3.5.14 Digital State Detection

The module must be able to detect the digital state of the LPMode and ModSelL signals. An I2C latch register in upper page 03 is latched on both rising and falling edges of the LPMode and ModSelL signals.

Address	Bit	Name	Description	Type
141 (page 03)	4	ModSelL transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
	5	LPMode transection		

3.5.15 Digital Control of IntL

During power-up of the module, IntL is defaulted to negated. The host can then set the status of this signal to any status through register 142 in upper page 03.

Address	Bit	Name	Description	Type
142 (page 03)	2	IntL control	00xb: Normal operation 010b: Force IntL to logic 0, VIntL < Vol(max) 011b: Force IntL to logic 1, VIntL > Voh(min) 1xxb: IntL is tri-stated	RW (NVR)
	1			
	0			

4 Connector Option Description

In case of **ML4062-LB2a-112-CON** Option, the module can either be inserted using the Pin Header or the Edge Connector.
With this option, the Electrical low-mph speed signals (IntL, LPMode, ResetL and ModselL) are not taken into consideration, and do not have any effect on the State Machine.
The module is always running in ModuleReady state on power up. You can only force the module to run in ModuleLowPwr state through register 26 bit 4 (ForceLowPwr). When this bit is set, the module is in low power mode, and all power spots are disabled. In order to re-activate power spots this bit should be cleared. Refer to section 3.5.3 for details.

5 High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by QSFP-DD800 MSA High Speed Electrical specs.
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 112 Gbps.

5.1 Insertion Loss Graph

The graph below shows the insertion loss simulated data of the **ML4062-LB2a-112**, for all eight channels.

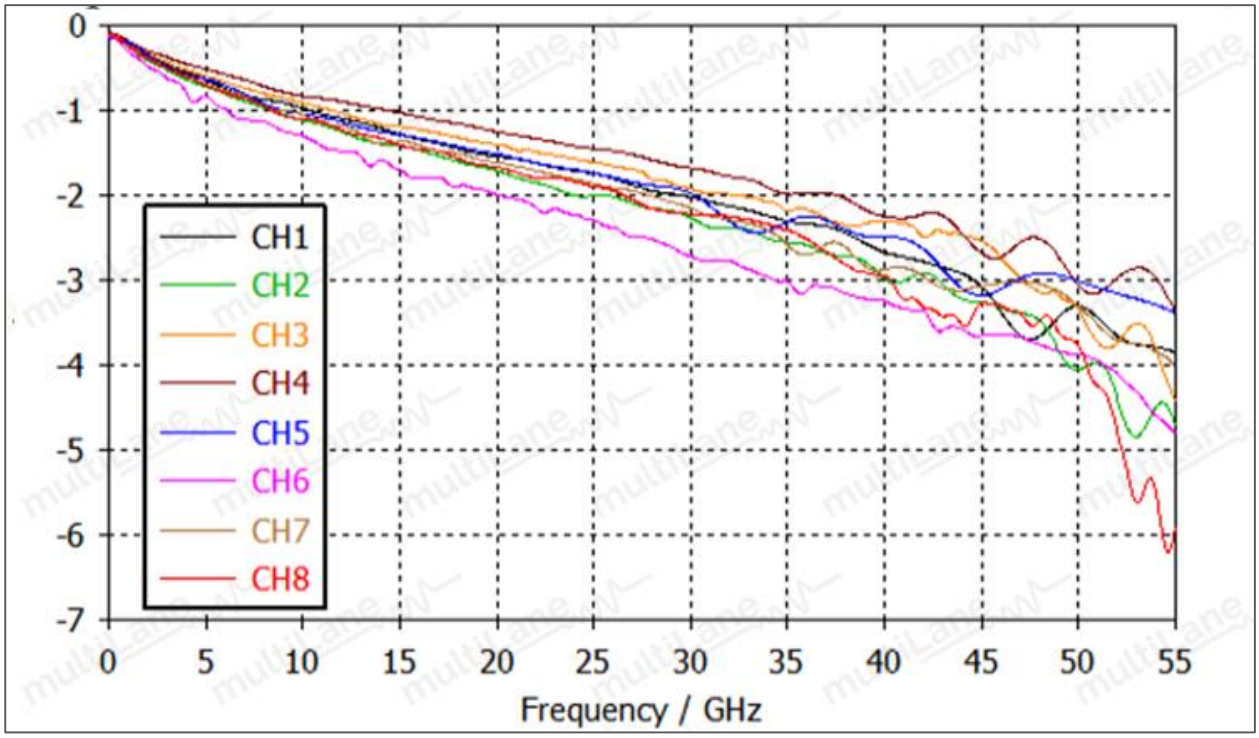


Figure 9: Insertion Loss Graph

6 QSFP-DD Pin Allocation

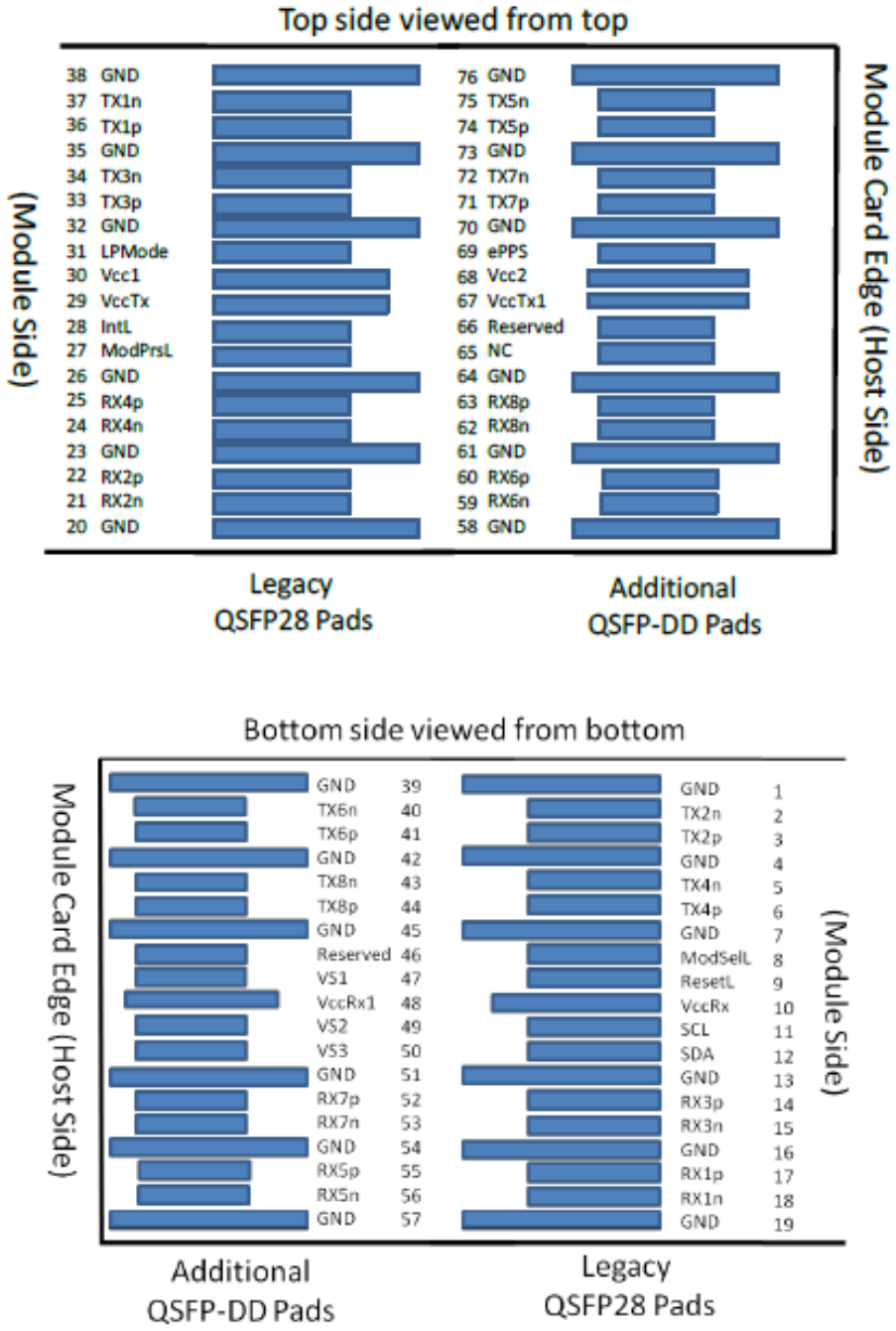


Figure 10: QSFP-DD Module Pad Layout

7 Mechanical Dimensions

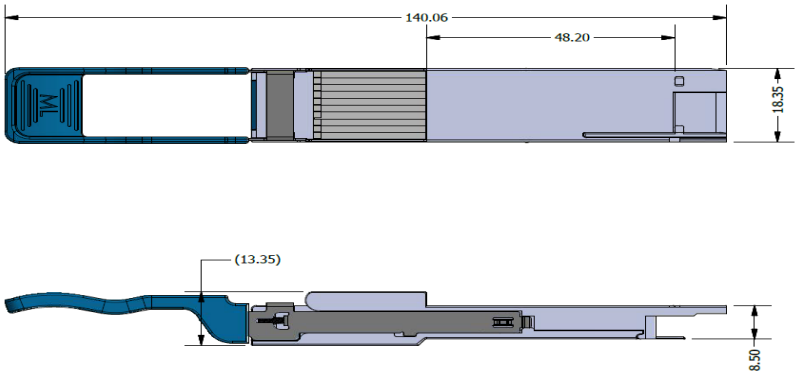


Figure 11: Mechanical Dimensions

8 Major FW Upgrades

Firmware upgrades are summarized in this section.

Revision History

Revision number	Date	Description
0.1	7/15/2020	▪ Preliminary
0.2	8/12/2020	▪ Add section 5.1: Insertion Loss Graph ▪ Update section 3.5.7: power spots distribution ▪ Update section 3.5.6: max measured current ▪ Update section 6: pin mapping diagram
0.3	10/7/2020	▪ Update section 3.5.7: power spots location
0.4	7/1/2021	▪ Update section 3.5.6: current sense limitation ▪ Update section 3.5.7: power spots control registers
0.5	3/23/2021	▪ Update nomenclature: from ML4062-TL2a-112 to ML4062-LB2a-112
0.6	6/3/2021	▪ Update section 3.5.12
0.61	6/28/2021	▪ Format updates and proofreading
0.7	2/14/2022	▪ Update section 3.3.3 : Update EEPROM content

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